

5. A PLL circuit according to any one of claims 1 through 4, wherein said control means is a means for switching an output of the phase comparator to a value at which an oscillation frequency of the voltage control oscillator decreases.

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B, 6. A PLL circuit according to any one of claims 1 through 4, wherein said control means is a means for switching a comparison signal inputted to the phase comparator such that an oscillation frequency of the voltage control oscillator decreases.